IDEC Chip Design Contest

A CMOS Resolution Reconfigurable Hybrid ADC for Bio-Signal Processing

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This circuit describes a CMOS reconfigurable hybrid ADC with high resolution for bio-signal processing. The proposed hybrid ADC consists of two exclusive parts, namely SAR architecture for MSB and Single Slope architecture for LSB. The reconfigurable capability was implemented by employing a timing block. The bit detection circuit driven by an external signal was able to reconfigure resolution (11 ~ 14-bit) of the proposed ADC. The proposed ADC was implemented with a standard CMOS 65nm 1-poly 6-metal process.

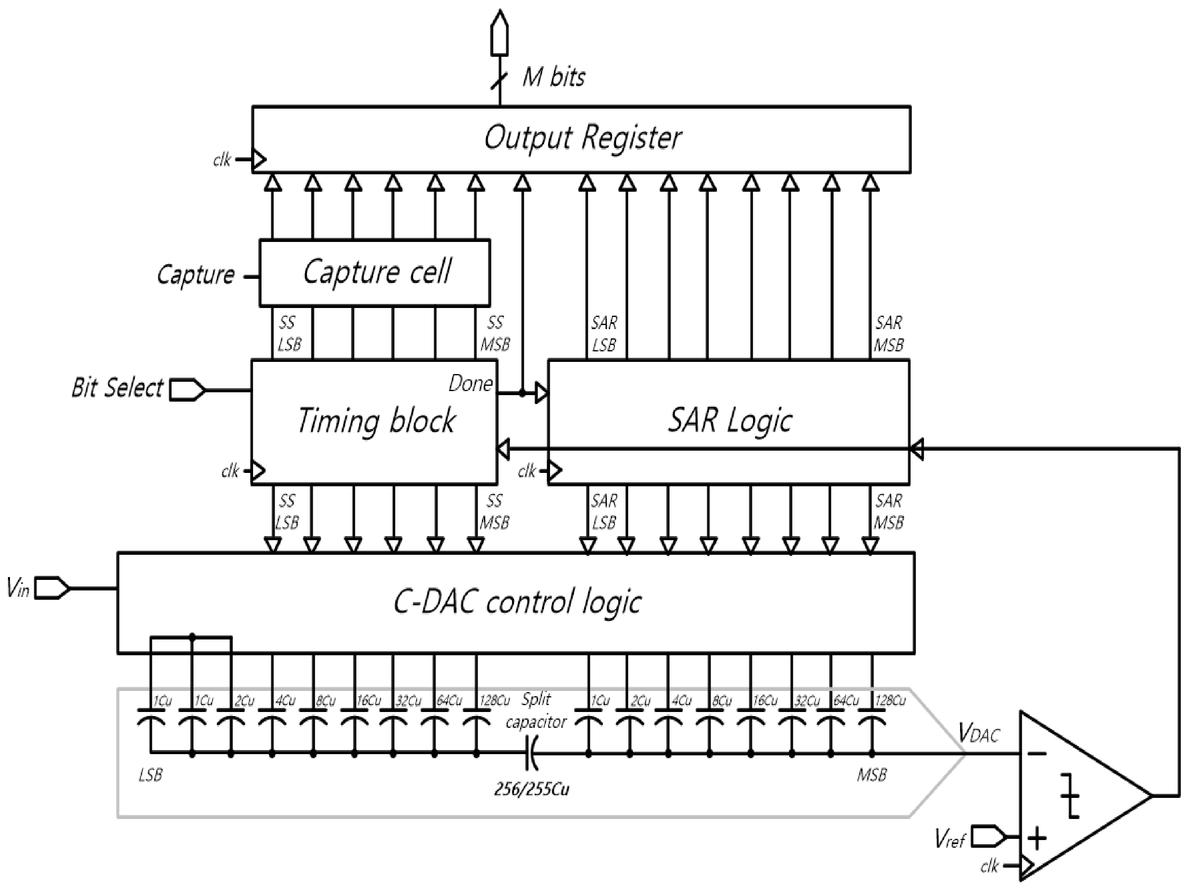

Fig 1.Top Cell

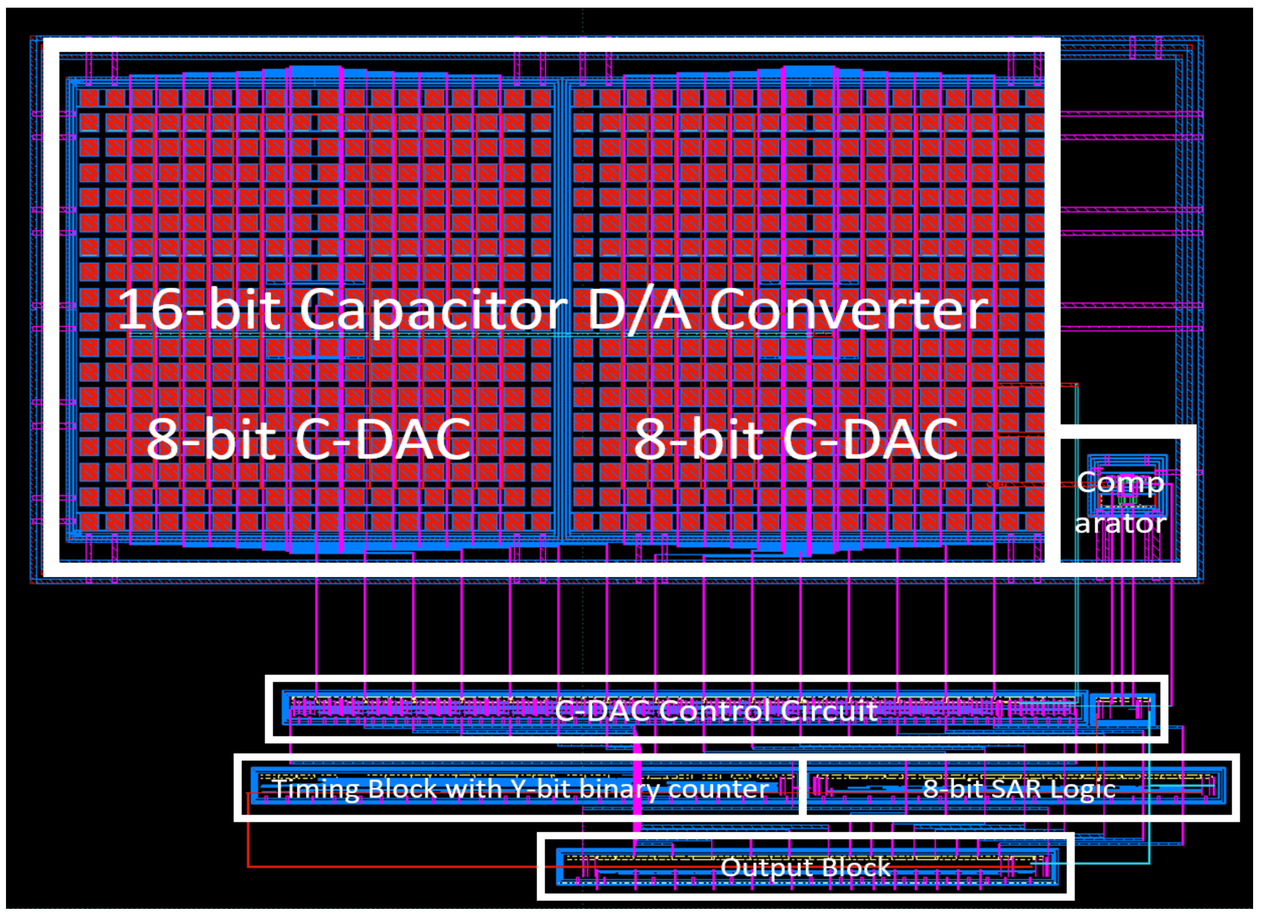

Fig 2.Top Cell Layout

the 8-bit SAR logic is connected to MSB 8-bit of C-DAC, and y-bit binary counter is connected to the remaining 8-bit of C-DAC. After the SAR logic completes activation, the binary counter starts to activate, elevates the output voltage of C-DAC with 1-LSB per one clock, and generates digital ramp starting from residue voltage of SAR ADC segments. The binary counter reconfigures the digital logic circuit within the counter to vary the resolution, ranging between 3 and 6. As the binary counter finishes its activation, the bit detection circuit generates Done signal which resets the overall circuits including the 10-clock counter with start-up circuit.

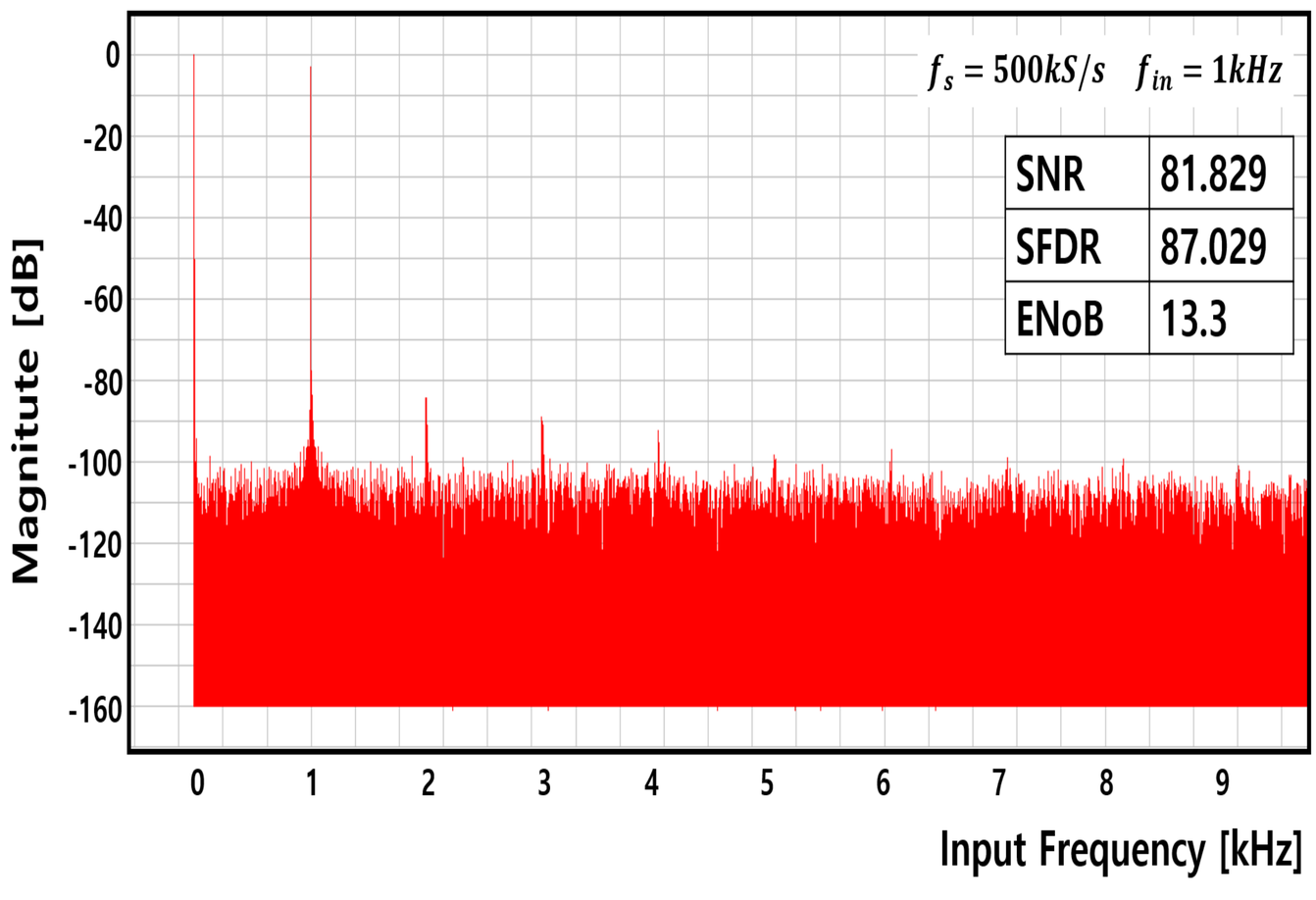

Fig 3. FFT simulation of 14bit Selected ADC

14bit Selected ADC FFT presented in Fig. 3 at the input and clock frequency of 1kHz and 500kHz shows SFDR, SNR, ENOB of 87dB, 81.8dB, and 13.3-bit, respectively.
The simulation results demonstrated power consumption of 81.8uW, ENOB of 13.3-bit, DNL/INL of ±0.7LSB and ±0.8LSB, FoM of 16.3 fJ/step, active layout area of 1700um x 500um.